METHOD AND APPARATUS FOR REDUCING LEAKAGE CURRENT IN AN SRAM ARRAY

ABSTRACT OF THE DISCLOSURE

A memory array including a bit cell row, a strap cell row, a first power supply line, and a first offset supply line is provided. The bit cell row may include a bit cell that includes a first transistor disposed in a first bit cell body region. The first transistor may include a first active region. The strap cell row may include a strap cell that includes a first strap cell body region. The first strap cell body region may be conductively coupled to the first bit cell body region. The first power supply line may be electrically coupled to the first active region and may provide a first supply voltage potential to the first active region. The first offset supply line may be electrically coupled to the first strap cell body region and may provide a first offset voltage potential to the first bit cell body region via the first strap cell body region. The first supply voltage potential is operable to be different from the first offset voltage potential.